IN THE SPECIFICATION:

Please amend the specification as follows:

Please amend the Brief Description of the Drawings section of the specification, beginning on Pg. 5, Line 7, as follows:

The above and further features, aspects, and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings in which:

Figure 1 is a conceptual block diagram of a phase locked loop in accordance with the principles of the invention;

Figure 2 is a conceptual block diagram of an illustrative digital embodiment of the new phase locked loop;

Figure 3 is a conceptual block diagram of an illustrative embodiment of the new phase locked loop that employs a beat detector to determine whether the frequency of an input signal lies outside the phase locked loop's lock range;

Figures 4A, 4B, 4C, 4D, and 4E respectively illustrate an example of an input signal whose frequency gradually increases until it lies outside the lock range of the PLL, the corresponding control voltage of the PLL's VCO, the output of the beat detector 126, the output of the beat period evaluator 128, and the output of the beat inhibit circuit;

Figure 5 is a graphical representation of the options available in selecting a requalification lock range; and

Figure 6 is a conceptual block diagram of a clock module that employs the new phase locked loop within a telecommunications system.

Figure 7 lists the time between transitions and corresponding frequency differences generated by comparing a variable frequency input signal to a 4 kHz reference signal.

Please amend the paragraph beginning on Pg. 8, Line 17, as follows:

In this illustrative embodiment the voltage output from the low pass filter 108 provides negative feedback to control the oscillator 110 and to thereby produce and

output signal PLLout which tracks the PLL input signal PLLin. The voltage output of the low pass filter is fed to an analog to digital converter (ADC) 120 which converts the low pass filter's voltage output into a digital value. Because the output of the ADC 120 is employed to control the oscillator 110, the ADC output is related to the frequency of the PLL output signal PLLout. Therefore, the controller [[104]] 105 may monitor the output of the ADC 120 to determine whether the frequency of the output signal PLLin is within its target range. The digital output of the ADC 120 is routed to the input of a digital to analog converter (DAC)122 where the value is converted to an analog signal. The output of the DAC 122 is fed to the voltage controlled oscillator 110 which produces the PLL output signal PLLout. The frequency of PLLout is a function of the DAC output voltage. The output signal PLLout is divided down by a divider 124 for convenience and the output of the divider 124 forms the signal to which the divided input signal from the divider 118 is compared. In this way, the output signal PLLout provides negative feedback to force the DAC output voltage to a value which produces an output signal from the VCO 110 that tracks the frequency of the input signal PLLin.

Please amend the paragraph beginning on Pg. 9, Line 3, as follows:

In operation, the controller 105, through control lines 123, controls the rate at which the ADC 120 and the DAC 122 operate in a manner which insures that excessive delays are not introduced into the loop and stable operation is maintained. Additionally, the controller [[104]] 105 monitors the digital output of the ADC 120. Whenever the controller detects a digital value that indicates that the input signal PLLin is outside a target frequency range, the controller [[104]] 105 takes corrective actions. These actions may include "freezing" the output of the DAC 122 or forcing the output of the DAC 122 to another value, such as that corresponding to the mid-range frequency of the VCO 110.

Please amend the paragraph beginning on Pg. 10, Line 7, as follows:

These transitions are input to the beat evaluator 128 which measures the time between transitions. Table 1, depicted in Figure 7, lists the time between transitions and

corresponding frequency differences generated by comparing a variable frequency input signal to a 4 kHz reference signal. The frequency difference is expressed in ppm off, a measure employed in telecommunications systems for which the new PLL is particularly well suited. The limits of acceptable performance for Stratum III and Stratum IV clocks are listed for reference purposes in the rightmost column.